REMARKS

I. Status of the Application

Prior to this Response, claims 1-18 were pending in the above-identified Application. By this Response, claims 1, 10, 11, and 14 are amended; claims 2-9, 12, 13, and 16-18 are unchanged from their respective immediate prior versions; claim 15 is canceled; and no claims are added. Thus, claims 1-14 and 16-18 are presently pending in the above-identified Application.

II. Claim Rejections - 35 U.S.C. § 102 (claims 1-18)

In the Office Action mailed on April 22, 2005, the Examiner rejected claims 1-18 under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 5,523,245 to Imai ("Imai").

A. Claims 11-18.

First, the rejection of claims 11-18 under 35 U.S.C. § 102(b) as allegedly anticipated by Imai has been traversed. It is well settled that to support a rejection for anticipation, the proffered reference must teach all features of the claimed invention. As to independent claim 11, the Examiner initially asserted that Imai's heavily doped p-type polysilicon layer 47 provided Applicants' claimed "base-terminal layer arranged on the semiconductor substrate." By this Response, Applicants have amended claim 11 (emphasis added) to point out that the recited base-terminal layer is "arranged on the semiconductor substrate without a sacrificial layer therebetween." As Applicants have discussed in the present Application, in an exemplary embodiment this feature facilitates V-shaped undercutting underneath a base-terminal layer 103 and makes for a lower profile transistor as well, among other things. E.g.,

Applicants' Specification at page 11, lines 16-33. Contrary to Applicants' amended claim 11, Imai teaches using a silicon oxide layer 46 (i.e., a sacrificial insulator) between its heavily doped p-type polysilicon layer 47 (i.e., its base-terminal layer) and its doped n-type epitaxial layer 43 (i.e., its semiconductor substrate). E.g., Imai at col. 5, lines 57-62 and at FIGs. 3A-3B. Thus, Imai clearly does not teach "a base-terminal layer arranged on the semiconductor substrate without a sacrificial layer therebetween" as recited in Applicants' amended claim 11.

Moreover, Applicants have further amended claim 11 (emphasis added) to additionally point out that in the recited invention "the base layer and the base-terminal layer are conductively connected essentially by means of a dopant diffused out of the base-terminal layer into the semiconductor substrate." This additional feature even further distinguishes Applicants' claimed invention from Imai. Contrary to Applicants' amended claimed 11, Imai teaches using a polysilicon layer 52 in a ring-shaped hollow space 51 to make a conductive connection between its p-type epitaxial base layer 53 (i.e., its base layer) and its p-type polysilicon layer 47 (i.e., its base-terminal layer). E.g., Imai at col. 6, lines 21-50 and at FIGs. 3A-3D. Imai teaches forming its ring-shaped hollow space 51 by sacrificially etching a portion of its silicon oxide layer 46. Id. Further, Imai teaches etching its polysilicon layer 52 into a ring-shaped polysilicon piece 52a and decreasing the resistivity of its polysilicon piece 52a by thermally diffusing the p-type impurity from its p-type polysilicon layer 47 into the polysilicon piece 52a. E.g., Imai at col. 6, lines 54-58. Thus, Imai clearly does not teach that "the base layer and the base-terminal layer are conductively connected essentially by means of a dopant diffused out of the base-terminal layer into the semiconductor substrate" as recited in Applicants' amended claim 11 (emphasis added), and much less does it teach such a

feature in combination with, as discussed above, "a base-terminal layer arranged on the semiconductor substrate without a sacrificial layer therebetween."

As to dependent claim 14, the Examiner initially asserted that Imai's recess 49 provided Applicants' claimed "further recess [comprising] an area which is arranged underneath the base-terminal layer." By this Response, Applicants have amended claim 14 (emphasis added) to point out that the recited further recess "comprises an area which extends laterally under the base-terminal layer." Extending Applicants' further recess laterally provides, among other things, additional area to improve Applicants' conductive connection of their base layer and base-terminal layer by diffusion of dopant from the base-terminal layer into the semiconductor substrate. Contrary to Applicants' amended claim 14, Imai merely teaches extending its further recess 49 axially and downwardly into its doped n-type epitaxial layer 43. E.g., Imai at FIGs. 3D-3F. Thus, Imai clearly does not teach a "further recess [comprising] an area which extends laterally under the base-terminal layer" as recited in Applicants' amended claim 14.

For at least the foregoing reasons, Imai does not teach all features of Applicants' invention as recited in amended independent claim 11 or amended dependent claim 14. Further, claims 12-14 and 16-18 all depend from claim 11 (either directly or indirectly) as a base claim and thus include all of the features that patentably distinguish Applicants' claimed invention over Imai as discussed above in connection with claim 11. Moreover, in addition to the features discussed above in connection with claim 11, claims 12, 13, and 16-18 include even additional features that patentably distinguish Applicants' claimed invention. Additionally, claim 15 has been canceled without prejudice or disclaimer of the subject matter therein.

Accordingly, the rejection of claims 11-18 under 35 U.S.C. § 102(b) as allegedly anticipated by Imai has been traversed, and Applicants respectfully request allowance of claims 11-14 and 16-18.

B. Claims 1-10.

Next, the rejection of claims 1-10 under 35 U.S.C. § 102(b) as allegedly anticipated by Imai has been traversed as well. To support a rejection for anticipation, the proffered reference must teach all features of the claimed invention. By this Response, Applicants have amended independent claim 1 (emphasis added) to point out that the claimed invention includes "forming a base-terminal layer on the substrate surface for providing a base terminal without a sacrificial layer therebetween . . . wherein a conductive connection between the base layer and the base-terminal layer is produced by diffusing a dopant out of the base-terminal layer into the semiconductor substrate." For the same reasoning as discussed above in connection with claim 11, Imai does not teach these features of Applicants' amended claim 1.

Additionally, by this Response Applicants have amended dependent claim 10 (emphasis added) to point out that the claimed step of etching a recess in the semiconductor substrate "comprises undercutting the base-terminal layer." For the same reasoning as discussed above in connection with claim 14, Imai does not teach this feature of Applicants' amended claim 10.

For at least the foregoing reasons, Imai does not teach all features of Applicants' invention as recited in amended independent claim 1 or amended dependent claim 10. Further, claims 2-10 all depend from claim 1 (either directly or indirectly) as a base claim and thus include all of the features that patentably distinguish Applicants' claimed invention over

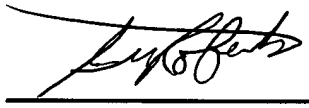
Imai as discussed above in connection with claim 1. Moreover, in addition to the features discussed above in connection with claim 1, claims 2-9 include even additional features that patentably distinguish Applicants' claimed invention.

Accordingly, the rejection of claims 1-10 under 35 U.S.C. § 102(b) as allegedly anticipated by Imai has been traversed, and Applicants respectfully request allowance of claims 1-10.

III. Conclusion

For at least the foregoing reasons, Applicants respectfully submit that all pending claims of the above-identified Application are in condition for allowance, and such action is respectfully requested. Additionally, Applicants respectfully request that if necessary to effect a timely response, this paper be considered as a Petition for an Extension of Time sufficient to effect a timely response, and any shortages in fees be charged, or any over payments in fees be credited to **deposit account No. 13-0014**.

Respectfully submitted,



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